**In the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims**

1-10. (Canceled).

11. (Currently Amended) A method for producing phase shifting layout data by a command script system that applies alt-PSM design rules, OPC, scattering bar rules, and gate blocking area generation comprising:

(a) identifying a single line transistor gate in an integrated circuit~~;~~;

(b) defining phase shifting areas for an alternating phase shifting mask (alt-PSM), said **alternating phase shifting mask** ~~phase mask~~ including said single line transistor gate and first opaque areas~~;~~;

(c) providing a layout including phase shifting areas in an opaque field and another layout of phase θ° or phase (180+θ) ° for said alt-PSM wherein θ is from 0 to 180~~;~~;

(d) assigning phase areas and **opaque gate block** ~~polygate~~ areas (true gate) for a gate block layer~~;~~;

(e) providing a layout for a tritone attenuated phase shift mask (att-PSM) including interconnects (poly layer excluding gates), **opaque gate** block ~~area~~ **areas** from (d), and sub-resolution scattering bars~~;~~; and

(f) processing the **layout** ~~layouts~~ for optical proximity corrections and outputting a

modified GDS layout for mask fabrication.

12. (Currently Amended)The method of claim 11 wherein said **alternating** phase **shift** mask is designed with a gate having a width and a length, said length is orthogonal to ~~the~~ two longer sides of an underlying active area layer, and said length is longer than the width of said active area **layer**.

13. (Currently Amended)The method of claim 11 wherein the ~~alternating~~ phase shifting areas include a set of θ phase and (180+θ)° phase regions, and each gate feature is adjacent to one θ° phase region and one (180+θ)° phase region.

14. (Original)The method of claim 13 wherein the phase shifting areas are comprised of chrome regions positioned between a θ° phase region and (180+θ)° phase region.

15. (Currently Amended)The method of claim 11 wherein from one to three full size scattering bars are positioned between chrome lines that are used to define shrunken gates and each **of the sub-resolution** scattering ~~bar~~ **bars** separates a θ° phase region from a (180+θ)°phase region.

16. (Currently Amended)The method of claim 15 wherein ~~the~~ **a** width of said scattering bars is equal to or greater than ~~the~~ **a** width of said chrome lines that define the shrunken gates and ~~the~~ phase widths of transparent regions adjacent to said chrome lines that define shrunken gates are the same as ~~the~~ phase widths adjacent to said scattering bars.

17. (Original)The method of claim 11 wherein said transistor gate comprises a single, substantially straight line in said layout.

18. (Currently Amended)The method of claim 11 wherein ~~said~~ **each** opaque gate block area includes phase shifting areas on the phase layout **in (e)** and polygate on active area and the size of said gate block area is demagnified somewhat on phase layouts to compensate for possible misalignment between first (alt-PSM) and second (att-PSM) masks.

19. (Original)The method of claim 11 wherein said attenuated regions in said att-PSM are used to define interconnect features having a width larger than said gate width.

20. (Currently Amended)The method of claim 19 wherein the **sub-resolation** scattering bars have a width from between 33% and 100% of the interconnect feature width and are separated from an interconnect feature by a distance that is from 1 to 2 times the width of said interconnect feature.

21-32. (Canceled).